REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-6, 9-19 and 28-30 are currently being prosecuted. Withdrawn claims 7, 8 and 20-27 have been cancelled. The Examiner is respectfully requested to reconsider his rejections in view of the Amendments and remarks as set forth below.

Claim for Priority

It is gratefully acknowledged that the Examiner has recognized Applicants' claim for foreign priority. However, the Examiner has indicated that none of the certified copies have been received. The Examiner is reminded that this is a PCT application and that the priority documents were filed in the international application.

Objection to the Drawings

The Examiner pointed out two objections in the drawings. First, the Examiner indicated that the reference character "12" has been used to designate two different items. According to the present amendment, Applicants have amended the specification on pages 17 and 18 in order to change the reference numeral for the circuits to "10." Figure 3 has likewise been amended to change the reference numeral in this figure. Accordingly, Applicants submit that this objection is overcome.

The Examiner also refers to the use of reference character 116 on page 8. However, it appears that the highest number utilized in the figures is 45 and that the reference character 116 has not been used at all. In particular, page 8, lines 1 and 17 have been examined and there is no

reference character 116 on those lines nor any reference to either the emitter polysilicon or film. It is believed that this objection is an error. Should the Examiner persist in this rejection, he is requested to explain wherein the problem lies.

Title

The Examiner objected to the title as not being descriptive. A new title has now been inserted which is directed to the claims.

Specification Headings

The Examiner pointed out that the incorrect headings have been utilized in the specification. Applicants have now changed some of the headings in the Specification in order to utilize standard U.S. prosecution headings.

Rejection Under 35 U.S.C. § 102

Claims 9, 11 and 12 stand rejected as being anticipated by Droz (5,399,847). The rejection is respectfully traversed.

The Examiner points out that the Droz reference shows an information carrier with a substrate 128 including an IC element 124, and an antenna coil 108 where the element is at the center portion of the substrate.

Applicants submit that the present invention is different from that shown in the reference. First, the present invention is a combination of elements including a coil integrally formed with

the IC element. This is different from the Droz arrangement where the element is separate from the coil and the coil is wound in a traditional manner around the carrier. It is this type of prior art device that the present application is trying to improve upon as discussed in the background of the invention.

Claim 9 has been amended to better bring out these differences by reciting a combination of elements including an IC element integrally formed with an antenna coil and disposed at a center portion of the substrate. Clearly, the Droz reference does not show a combination with the antenna coil formed integrally with the IC element. Further, the claim now makes it clear that both the IC element and the antenna are disposed at a center portion of the substrate. This is clearly not the case in the Droz reference where the coil is made into a circle around the outer portions of the carrier. Applicants have also re-worded the last phrase of claim 9 to make this more clear. In particular, the language used now follows that of the specification at page 28, line 25.

Applicants submit that the Droz reference does not show a combination of elements including an IC element formed integrally with the antenna coil, nor does it show that both the antenna coil and IC element are at the center portion of the substrate. Accordingly, Applicants submit that claim 9 defines thereover.

Rejection Under 35 U.S.C. § 103

Claims 1-6, 14 and 15 stand rejected under 35 USC §103 as being obvious over Droz et al. in view of Shindo et al (5,048,179). This rejection is respectfully traversed. In regard to claim 1, the Examiner admits that Droz et al fails to show the various metal layers of the

conductor used in the coil. However, the Examiner states that since the method of making the layers is a process, these limitations are not considered. Applicants submit that even if the method for making layers is not considered, the claim recites a combination including a conductor having a multi-layer structure.

The Examiner relies on the Shindo et al reference to show the use of aluminum, copper and chromium to provide electrical connection among components. However, the disclosure of these materials on column 5, line 7-11 of the reference merely state that any electrically conductive material, including an alloy of aluminum, copper, chromium and gold may be used in place of aluminum. The reference does not teach the use of multi-layer conductors. Finally, Applicants submit that even if the teachings of Shindo et al are added to Droz, it still does not teach the limitations presently defined in claim 1.

Claims 2-6 depend from claim 1 and as such are also considered to be allowable. These claims further include other features regarding the conductor making up the coil so that these claims would be additionally allowable.

Likewise, claims 14-15 depend from claim 9 and as such are considered to be allowable. These claims recite additional features of the information carrier and are likewise additionally allowable.

Claims 10 and 19 stand rejected as being obvious over Droz et al in view of Masahiko (5,852,289). Claim 13 stands rejected as being obvious over Droz et al in view of Parmentier (4,483,067). Claims 16-18 stand rejected as being obvious over Droz et al in view of Fidalgo (5,598,032). These rejections are respectfully traversed. Applicants submit that these claims are allowable based on their dependency from allowable claim 9, as well as for the additional

combinations of limitations set forth therein. Reconsideration and withdrawal of these rejections are respectfully requested.

New Claims

Applicants are also submitting herewith three new claims to include further limitations not seen in the references. Claim 28 describes that the resistance of the metal-plated layer is less than resistance of the other layer. This is not seen in any of the references. Claims 29 and 30 describe the mounting of the antenna coil entirely on the integrated circuit element. In the present invention, the entire device is mounted on a single chip. This is not seen in the references where the coil is formed separately from the chip and is merely connected thereto. Accordingly, these claims are believed to be additional allowable.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Robert F. Gnuse (Reg. No. 27,295 at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicants respectfully petition for a three (3) month extension of time for filing a reply in connection with the present application, and the required fee of $920.00 is attached hereto.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title

The title has been amended as follows:

[DEVICE AND ITS PRODUCTION METHOD, AND INFORMATION CARRIER MOUNTED WITH IC DEVICE AND ITS PRODUCTION METHOD] **IC COIL MOUNTED IN AN INFORMATION CARRIER**

In the Specification

The subtitle beginning on Page 1, line 1 has been amended as follows:

--BACKGROUND OF THE INVENTION

Field of the Invention--

The subtitle before the paragraph on Page 1, line 8 has been amended as follows:

--DESCRIPTION OF RELATED ART--

The subtitle before the paragraph on Page 3, line 17 has been amended as follows:

--SUMMARY OF THE INVENTION--

The subtitle before the paragraph on Page 13, line 3 has been amended as follows:

--DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--

The paragraph beginning on page 17, line 12 has been amended as follows:

--As shown in Fig. 3, a large number of circuits [12] 10 for the IC element are formed with equidistance in an inner portion exclusive of the outermost peripheral portion, wherein the surface passivation film 2 is formed over the surface on which the circuit for the IC element are formed (see Figs. 4 and 5).--

The paragraph beginning on page 17, line 19 has been amended as follows:

--In the IC element manufacturing method according to a first exemplary embodiment shown in Figs. 4A, 4B, 4C, 4D, 4E and 4F, the metal-sputtered layer or alternatively metal-evaporated layer 6 is formed uniformly on the surface passivation film 2 deposited on the circuit-formed surface of the finished wafer 11 by using aluminum or an aluminum alloy or alternatively copper or a copper alloy, as shown in Fig. 4A. Subsequently, a photoresist layer 12 is uniformly formed on the metal-sputtered layer or alternatively metal-evaporated layer 6 and then the photoresist layer as formed is covered with a mask 13 of a required pattern inclusive of the coils, whereon the photoresist layer 12 is exposed to illumination of light rays 14 of a predetermined wavelength externally of the mask 13, as is shown in Fig. 4B. Thereafter, the photoresist layer 12 undergone the light exposure is subjected to a developing process, whereby the light-exposed portions of the photoresist layer 12 are removed, as a result of which the portions of the metal-sputtered layer or alternatively metal-evaporated layer 6 which correspond to the above-mentioned light exposure pattern is exposed outwardly, as is shown in Fig. 4C. The exposure pattern of the metal-sputtered layer or alternatively metal-evaporated layer 6 includes a ring-shaped electrode portion 15, the antenna coils 3 formed on the portions opposite to the aforementioned circuits [10] 12, respectively, and lead portions 16 for connecting the individual antenna coils 3 and the electrode portion 15, as is shown in Fig. 6. In succession, by making use of the above-mentioned electrode portion 15 as one electrode, electroplating or precision electroforming process is performed on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, or thereby laminate the metal-plated layers 7 on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, as shown

in Fig. 4D. Subsequently, the photoresist layer 12 deposited on the surface of the finished wafer 11 is removed through an ashing or the like process to thereby obtain the finished wafer 11 formed with the metal-plated 7 including the electrode portion 15, the antenna coils 3 and the lead portions 16 deposited on the uniform metal-sputtered layer on alternatively metal-evaporated layer 6, as shown in Fig. 4E. In succession, the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed through the metal-plated layer 7 is selectively etched to thereby remove the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed externally through the metal-plated layer 7, as is shown in Fig. 4F. Thus, there is obtained the finished wafer 11 on which both the metal-sputtered layer or alternatively metal-evaporated layer 6 and the metal plated layer 7 are formed in the required conductive pattern shown in Fig. 6. Finally, the finished after 11 mentioned just above is scribed to obtain the desired IC elements 1 shown in Fig. 1.--

In the Claims

Claims 7, 8 and 20-27 have been cancelled.

Claims 1- 6 and 9-19 have been amended as follows:

1. (Amended) An IC element formed integrally with a coil for performing contactless data communication with external equipment, [characterized in that] <u>comprising:</u>

a conductor constituting said coil [is] implemented in a multilayer structure including a metal-sputtered layer or alternatively a metal-evaporated-layer and a metal-plated layer.

2. (Amended) [An] The IC element as set forth in claim 1, [characterized in that] wherein said metal-sputtered layer or alternatively said metal-evaporated layer is formed of at least one metal of aluminum, nickel, copper and chromium or alternatively an alloy containing those metals, and [that] said metal-plated layer deposited on said metal-sputtered layer or alternatively said metal-evaporated layer is formed of copper.

3. (Amended) [An] The IC element as set forth in claim 1, [characterized in that] wherein said coil is formed on a surface of said IC element formed with input/output terminals with interposition of an electrically insulative surface passivation film and [that] the input/output terminals of said IC element and said coil are electrically interconnected through through-holes formed in said surface passivation film and each having a diameter smaller than a line width of said coil.

4. (Amended) [An] The IC element as set forth in claim 1, [characterized in that] wherein said coil is implemented in a rectangular spiral pattern in a planar shape and [that] all or some of corner portions of said rectangular spiral pattern are chamfered.

5. (Amended) [An] The IC element as set forth in claim 1, [characterized in that] wherein said metal-plated layer is formed by resorting to [a] an electroless plating method or alternatively an electroplating method or alternatively a precision electroforming method.

6. (Amended) [An] The IC element as set forth in claim 1, [characterized in that] wherein a line width of said coil is not smaller than 7 μm, an inter-line distance thereof is not greater than 5 μm and the number of turns thereof is not smaller than 20 turns.

9. (Amended) An information carrier [including] comprising:

a substrate having an IC element mounted thereon [an IC element],

said IC element formed integrally with an antenna coil for performing data communication in a contactless manner with external equipment,

[characterized in that] said IC element [is] and said antenna coil being disposed at a center portion of said substrate as viewed in a planar direction perpendicularly to a plane of said substrate.

10. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein both of top and bottom surfaces of said IC element are covered with said substrate.

11. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein only one surface of said IC element is covered with said substrate.

12. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein said substrate is formed in a circular or square planar shape.

13. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein said substrate is wholly or partially formed of paper.

14. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein said substrate is implemented in a three-bonded-layer structure including a top member, a bottom member and an intermediate member, and [that] said IC element is accommodated within a through-hole formed in said intermediate member at a mid portion thereof.

15. (Amended) [An] The information carrier as set forth in claim 14, [characterized in that] wherein said [though] through-hole is formed circularly in a planar shape.

16. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein said substrate is implemented in a two-bonded-layer structure including a top member and a bottom member, and [that] said IC element is accommodated within a recess formed in said top member or alternatively in said bottom member at a mid portion thereof.

17. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] wherein said substrate is implemented in a single layer structure, and [that] said IC element is accommodated within a recess formed in said substrate at a mid portion thereof.

18. (Twice Amended) [An] The information carrier as set forth in claim 16, [characterized in that] wherein said recess is formed circularly in a [plane] planar shape.

19. (Amended) [An] The information carrier as set forth in claim 9, [characterized in that] further comprising another discrete coil which is separately formed independent of said IC element internally of said substrate.

Claims 28-30 have been added.